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PATENT & TRADEMARK OFFICE

DOCKET NO. P04761 **PATENT**
CLIENT NO. NATI15-04761
Customer No. 23990

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	John E. Gavlik, et al.
Serial No.:	09/713,389
Filed:	November 15, 2000
For:	NETWORK INTERFACE CARD USING PHYSICAL LAYER MICROCONTROLLER AND METHOD OF OPERATION
Group No.:	2157
Examiner:	Hussein A. El-Chanti

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated in the arguments below, demonstrating the clear legal and factual deficiency of the rejections of some or all claims.

The Office Action rejects Claims 1-5, 8-13, 16-21 and 24 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,781,773 to Johnston et al. ("Johnston").

Johnston describes an industrial controller permitting program editing during program execution, by placing new instructions in a second memory area, then placing conditional jump instructions to integrate the new instructions into the pre-existing program. Johnston does not teach or suggest the limitations of independent Claims 1, 9, and 17. Examiner El-Chanti has never actually indicated which elements he believes satisfy each of the claim limitations, despite Applicant's request that he do so, instead referring to large passages of Johnson, so it is unclear where exactly the Examiner's misapprehension lies.

Claim 1 requires an apparatus for controlling a physical layer interface of a network interface card. Johnston does not so much as mention a network, or a network interface card, or a physical layer interface. The rejection of claim 1 is legally and factually deficient.

Claim 1 also requires a read only memory (ROM) capable of storing an embedded control program. Johnston teaches that memory unit 54 includes ROM (col. 5, lines 46-47) and that the processor 62 reads instructions of the relay ladder logic diagram from memory (col. 6, lines 1-3). The rejection of claim 1 is legally and factually deficient.

Claim 1 also requires a random access memory capable of storing a downloadable software control program downloaded from an external processing system. Johnston teaches that edited relay ladder instructions can be "entered by the user or by accessing a pre-stored file" (col. 8 lines 52-53). Nothing in this passage teaches storing a downloadable software control program downloaded from an external processing system. In particular, Johnston is silent as to where the "pre-stored filed" is

stored or how it is entered. The rejection of claim 1 is legally and factually deficient.

Claim 1 also requires a microcontroller capable of controlling the physical layer interface, wherein said microcontroller in a first operating mode is capable of executing said embedded control program to thereby control said physical layer interface. Johnston does not teach or suggest a microcontroller capable of controlling a physical layer interface of a network interface card, as claimed. Johnston does not teach or suggest that the relay ladder logic diagram is in any way capable of controlling a physical layer interface of a network interface card, as claimed. The rejection of claim 1 is legally and factually deficient.

Claim 1 also requires that the microcontroller in a second operating mode is capable of executing said downloadable software control program in place of said embedded control program to thereby control said physical layer interface. Johnston does not teach or suggest this feature. Even assuming *arguendo* that the "new instructions" qualified as the claimed "downloadable software control program", these new instructions are never executed "in place of said embedded control program", as claimed. Instead, when the edit is complete, jump and branch instructions are added specifically to "integrate [the new instructions] into the pre-existing program" (col. 9, lines 20-21). That is, the pre-existing program executes without modification until the new instructions are integrated into the pre-existing program. There is no "first operating mode" where the pre-existing instructions are executed and a "second operating mode" where the new instructions are executed in place of the pre-existing instructions, as claimed.

Examiner El-Chanti responds that these claim limitations are "optional", and so gives them no weight. On the contrary, the claim specifically requires that the microcontroller have specific

capabilities. Nothing in Johnston teaches or suggests these capabilities. As Examiner El-Chanti has effectively conceded that he has ignored these limitations, the rejection of claim 1 is legally and factually deficient.

Claim 1 also requires that the microcontroller comprises a plurality of control registers capable of controlling said first and second operating modes, wherein said microcontroller switches from said first operating mode to said second operating mode when said external processing system stores a jump address to said RAM in a first one of said plurality of control registers. This feature is not taught or suggested by Johnston. Johnston does not teach, suggest, discuss, or even mention registers at all.

Independent Claim 9 includes many limitations similar to those of claim 1, and so the arguments above apply to Claim 9 as well. In addition, Claim 9 requires a hard disk drive, which is not taught or suggested by Johnston at all. Claim 9 requires that the hard disk drive be capable of storing a network interface card (NIC) configuration file containing a downloadable software control program; Johnston does not teach or suggest anything like a network interface card (NIC) configuration file.

Independent Claim 17 requires in a first operating mode, executing an embedded control program stored in a read only memory (ROM) coupled to the microcontroller to thereby control the physical layer interface. This limitation is not taught or suggested by Johnston for reasons described above with relation to the claimed physical layer interface. The rejection of claim 9 is also legally and factually deficient.

The rejections of all claims are legally and factually deficient.

CONCLUSION

As a result of the foregoing, the Applicant asserts that the claims in the Application are in condition for allowance over all art of record, and respectfully requests this case be returned to Examiner Tran for allowance or, alternatively, further examination.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK BUTRUS P.C.

Date: May 1, 2006

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CERTIFICATE OF MAILING BY FIRST CLASS MAIL

Sir:

The undersigned hereby certifies that the following documents:

1. Notice of Appeal;
2. Request for 1 mo. Extension of Time (in duplicate);
3. Pre-Appeal Brief Request for Review;
4. Fee Transmittal for FY 2006 (in duplicate);
5. Check in the amount of $620.00 for the Notice of Appeal filing fee($500) and Extension Fee ($120); and
6. Postcard receipt.

relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to MAIL STOP AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 1, 2006.

Date: May 1, 2006 Mailer

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